PXIe-63987

PXI Express Embedded
Controller
User's Manual

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Leading **EDGE COMPUTING**

Preface

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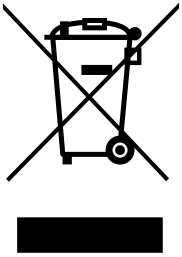
Environmental Responsibility



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Battery Labels (for products with battery)

California Proposition 65 Warning

WARNING: This product can expose you to chemicals including acrylamide, arsenic, benzene, cadmium, Tris(1,3-dichloro-2-propyl) phosphate (TDCPP), 1,4-Dioxane, formaldehyde, lead, DEHP, styrene, DINP, BBP, PVC, and vinyl materials, which are known to the State of California to cause cancer, and acrylamide, benzene, cadmium, lead, mercury, phthalates, toluene, DEHP, DIDP, DnHP, DBP, BBP, PVC, and vinyl materials, which are known to the State of California to cause birth defects or other reproductive harm. For more information go to www.P65Warnings.ca.gov.

Trademarks

Product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

Conventions

Take note of the following conventions used throughout this manual to make sure that users perform certain tasks and instructions properly.

 NOTE:	Additional information, aids, and tips that help users perform tasks.

 CAUTION:	Information to prevent ***minor*** physical injury, component damage, data loss, and/or program corruption when trying to complete a task.

 WARNING:	Information to prevent ***serious*** physical injury, component damage, data loss, and/or program corruption when trying to complete a specific task.

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1 Introduction

The JYTEK PXIe-63987 PXI Express™ embedded controller is based on the seventh generation Intel® Core™ i7 processor specifically designed for PXI Express-based testing systems. A rugged and stable operating environment is provided for a variety of testing and measurement applications.

Combining state-of-the-art Intel® Core™ i7-7820EQ 3.0GHz processors and up to 32GB of DDR4 2400MHz memory, the PXIe-63987 utilizes four separate computing engines on a single processor, enabling execution of four independent tasks simultaneously. With a configurable PCIe switch, the PXIe-63987 can support four links x4 or two links x8 x16 PXI Express link capability, with maximum system throughput of up to 16GB/s (PCI Express 3.0).

PXI Express-based testing systems typically make up a PXI Express platform and diversified standalone instruments for complex testing tasks. The PXIe-63987 series provides ample interfaces, including two DisplayPort connectors, allowing connection to two monitors, dual USB 3.0 connections for high speed peripheral devices, dual Gigabit Ethernet ports, one for LAN connection and the other for controlling LXI instruments, four USB 2.0 ports for peripheral devices and USB instrument control, an SMB connector for configurable input/output routing of signal to/from PXI Trigger Bus on PXI Express chassis, and a Micro-D GPIB connector for GPIB instrument connection, for hybrid PXI-based testing system control.


NOTE:

Memory addressing over 4GB is OS-dependent, such that a 32-bit operating system may be unable to address memory space over 4GB. To fully utilize memory, 64-bit operating systems are required.

1.1 Features

- PXI™-5 PXI Express Hardware Specification Rev.1.0
- Intel® Core™ i7-7820EQ processor for maximum computing power, 3.7GHz maximum in single-core, Turbo Boost mode.
- Dual Channel DDR4 SODIMM
  - Up to 32GB 2400MHz
- Maximum System Throughput 16GB/s
- PXI Express Link Capability
  - Four Links Configuration: x4 x4 x4 x4
  - Two Links Configuration: x16 x8
- Pre-integrated SATA solid state drive at 240GB
  - Supports 2.5” HDD or SSD
  - SATA 6.0 Gb/s
  - Supports AHCI
- Integrated I/O
  - Dual Gigabit Ethernet ports
  - Two USB 3.0 Ports
  - Four USB 2.0 Ports
  - Built-in GPIB (IEEE488) controller
  - Dual DisplayPort connectors
  - One COM port (D-sub9 serial)
  - Trigger I/O for advanced PXI™ trigger functions
- OS
  - Microsoft Windows 10 64 bit

1.2 Specifications

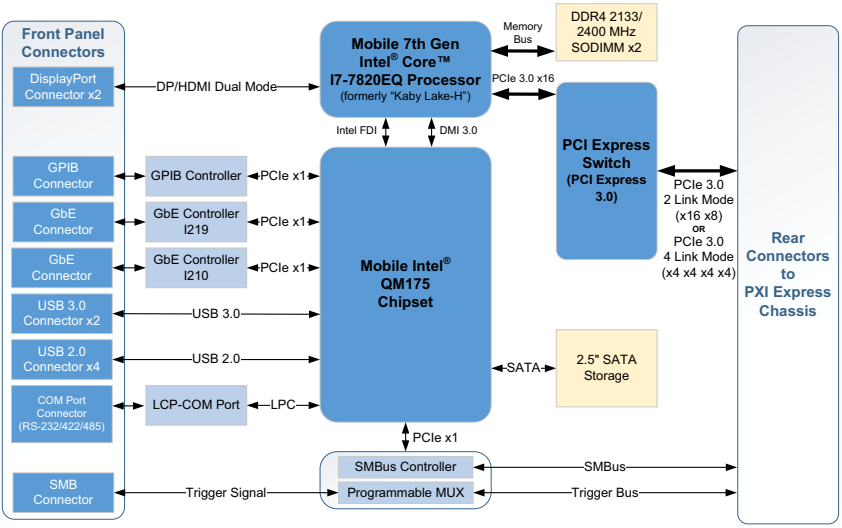


Figure 1-1: PXIe-63987 Functional Block Diagram

Processor

- Intel® Core™ i7-7820EQ 3.0GHz processor
- DMI (Direct Media Interface) 3.0 with 8GT/s bandwidth in each direction

Chipset

Mobile Intel® QM175 chipset

Memory

- Two standard 260-pin DDR4 SODIMM sockets
- Supports 2133/2400MHz RAM up to 32 GB total
- Supports non-ECC, unbuffered memory


NOTE:

The externally accessible SODIMM socket can accept replacement DDR4 DRAM DIMM modules.
PXIe-63987 specifications and stability guarantees are only supported when JYTEK-provided DDR4 DRAM SODIMM modules are used.

Video

- DisplayPort supports up to 3840x 2160 @ 60 Hz resolution
- DVI (with passive DisplayPort-to-DVI adapter) supports resolution up to 1920 x 1200 @ 60 Hz


NOTE:

DisplayPort adapters for other standards are available, with maximum available resolution dependent on the adapter chosen

Hard Drive

Built-in 2.5” 500GB SATA hard drive or 240GB SATA solid state hard drive.

I/O Connectivity

Dual Gigabit Ethernet controllers through two RJ-45 connectors with speed/link/active LED on the faceplate, with both supporting Wake on LAN.

USB

Four USB 2.0 and two USB 3.0 ports on the faceplate.

GPIB

Onboard IEEE488 GPIB controller through Micro-D 25-pin connector on the faceplate.

Trigger I/O

One SMB connector on the faceplate to route an external trigger signal to/from PXI trigger bus

Dimensions (3U PXI module)

3U/4-slot PXI standard

Weight

1.0 kg (exclusive of packaging)

Environmental

Operating temperature with SSD	0 to 55°C
Operating temperature with HDD	0 to 50°C
Storage temperature	-20 to 70°C
Relative humidity , non-condensing	5 to 95%

Shock and Vibration

Functional shock 30 G, half-sine, 11 ms pulse duration

Random vibration:

- Operating 5 to 500 Hz, 0.21 Grms, 3 axes
- Non-operating 5 to 500 Hz, 2.46 Grms, 3 axes


NOTE:

Environmental & Shock and Vibration values are only guaranteed with use of an JYTEK-provided SSD/HDD

Certification

Electromagnetic compatibility:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55032 2015/AC: 2016 Class A
- EN 55032 2015/AC: 2016 Class B
- EN 55024 2010+ A1: 2015
- EN 61000-3-2:2014 : Class A
- EN 61000-3-3:2013 : Class A
- EN 55024:2010+A1:2015 : Immunity
- FCC 47 CFR Part 15 Subpart A (Class A)
- FCC 47 CFR Part 15 Subpart B (Class B)
- ICES-001 Class A
- ICES-003 Issue 6-2016
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 32: 2015 (Ed 2.0)/C1:2016 : Class B

The PXIe-63987 meets the essential requirements of applicable European Directives.

Power Requirements

Typical Consumption	DC +3.3V	DC +5V	DC +12V
Typical operation (Measured while W10 is idle)	5A	2.5A	2A
Heavy operation (Measured while W10 is under heavy CPU and storage utilization)	5A	2.8A	8A

1.3 I/O and Indicators

1.3.1 Front Panel

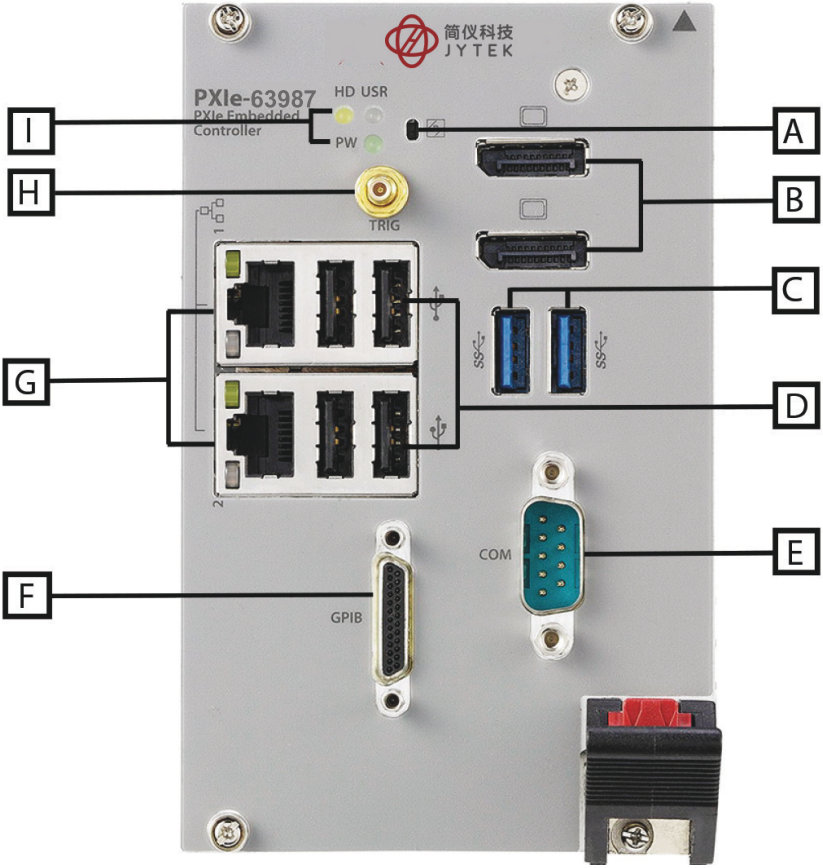


Figure 1-2: PXIe-63987 Front Panel

A	Reset Button	F	GPIB Connector (Micro D-Sub 25P)
B	2X DisplayPort	G	2X Gigabit Ethernet
C	2X USB 3.0	H	PXI Trigger
D	4X Type-A USB 2.0	I	LED indicators
E	COM port (D-sub9 serial)		

Table 1-1: Front Panel Legend

PXI Trigger Connector

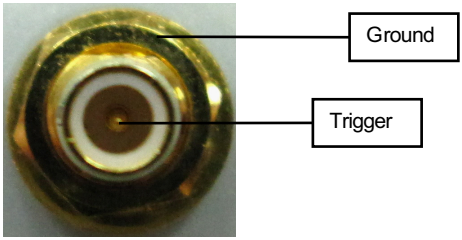


Figure 1-3: PXI Trigger SMB Jack

The PXI trigger connector is a SMB jack, used to route external trigger signals to or from the PXI backplane. Trigger signals are TTL-compatible and edge sensitive. The PXIe-63987 provides four trigger routing modes from/to the PXI trigger connector to synchronize PXI modules, including

- From a selected trigger bus line to PXI trigger connector
- From the PXI trigger connector to a selected trigger bus line
- From software trigger to a selected trigger bus line
- From software trigger to PXI trigger connector

All trigger modes are programmable by the provided driver.

DisplayPort Connectors

Provide monitor connection, with, if connecting to VGA/DVI/HDMI monitors, installation of requisite adapters required. Dual display function is also supported.

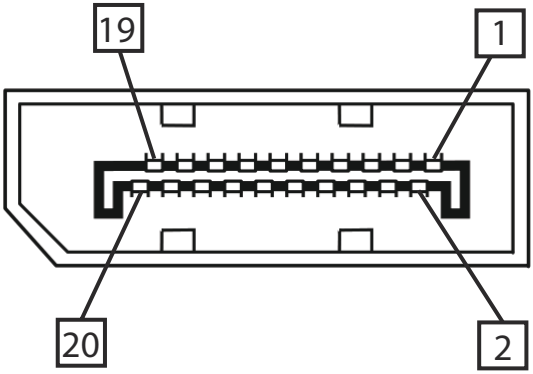


Figure 1-4: DisplayPort Connector

Pin	Signal	Pin	Signal
1	CN_DDPx0+	11	GND
2	GND	12	CN_DDPx3-
3	CN_DDPx0-	13	CN_DDPx_AUX_SEL
4	CN_DDPx1+	14	CN_DDPx_CONFIG2
5	GND	15	CN_DDPx_AUX+
6	CN_DDPx1-	16	GND
7	CN_DDPx2+	17	CN_DDPx_AUX-
8	GND	18	CN_DDPx_HPD
9	CN_DDPx2-	19	GND
10	CN_DDPx3+	20	+V3.3_DDPx_PWR

Table 1-2: DisplayPort Pin Assignment

1.3.2 GPIB Connector

The GPIB connector on PXIe-63987 is a micro D-sub 25P connector, controlling external bench-top instruments. Connection to other instruments requires the optional ACL-IEEE488-MD1-A cable. The on-board GPIB controller provides:

- Full compatibility with IEEE 488 standard
- Up to 1.5MB/s data transfer rates
- Onboard 2 KB FIFO for read/write operations
- Driver APIs are compatible with NI-488.2 driver software
- Connection with up to 14 instruments

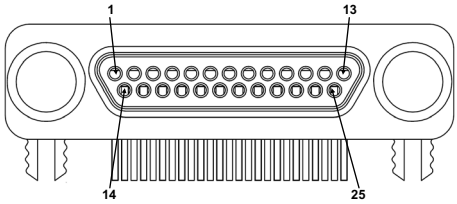


Figure 1-5: GPIB Connector

Pin	Signal	Description	Pin	Signal	Description
1	DIO1#	GPIB Data 1	14	DIO5#	GPIB Data 5
2	DIO2#	GPIB Data 2	15	DIO6#	GPIB Data 6
3	DIO3#	GPIB Data 3	16	DIO7#	GPIB Data 7
4	DIO4#	GPIB Data 4	17	DIO8#	GPIB Data 8
5	EOI	End Or Identify	18	REN	Remote Enable
6	DAV	Data Valid	19	Ground	Signal Ground
7	NRFD	Not Ready For Data	20	Ground	Signal Ground
8	NDAC	No Data Accepted	21	Ground	Signal Ground
9	IFC	Interface Clear	22	Ground	Signal Ground
10	SRQ	Service Request	23	Ground	Signal Ground
11	ATN	Attention	24	Ground	Signal Ground
12	Chassis Ground	Chassis Ground	25	Ground	Signal Ground
13	Ground	Signal Ground			

Table 1-3: GPIB Pin Description

1.3.3 Reset Button

The reset button, activated by insertion of any pin-like implement, executes a hard reset for the PXIe-63987.

1.3.4 LED Indicators

Three LED indicators on the faceplate indicate operational status of the PXIe-63987, as follows.

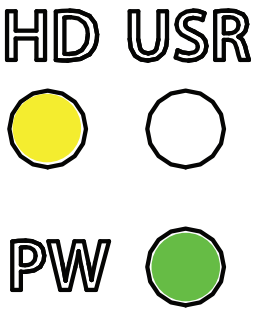


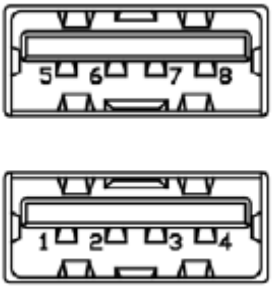
Figure 1-6: PXIe-63987 LED Indicators

LED	Color	Description
PW	Green	Indicates system power, remaining lit when the system boots normally and main power supply is functioning
HD	Yellow	Indicates operating state of the HDD or SSD, flashing during access to or activity on the SATA HDD.
USR	Blue	User-programmable LED indicator

Table 1-4: LED Indicator Legend

1.3.5 USB 2.0 Ports

The PXIe-63987 provides four USB 2.0 ports via USB Type A connectors on the faceplate, all compatible with hi-speed, full-speed and low-speed USB devices. Supported boot devices include USB flash drive, USB floppy, USB CD-ROM, and others, with boot priority and device settings configurable configured in BIOS. Please see Section B.5.1: Boot Configuration for more information.



Pin	Signal
1/5	Power 5V
2/6	USB Data-
3/7	USB Data +
4/8	Ground

Table 1-5: USB 2.0 Port Pin Assignment

1.3.6 Gigabit Ethernet Ports

Dual Gigabit Ethernet connection is provided on the PXIe-63987 front panel.

Pin	1000Base-T Signal	100/10Base-T Signal
1	MDI0+	TX+
2	MDI0-	TX-
3	MDI1+	RX+
4	MDI2+	Reserved
5	MDI2-	Reserved
6	MDI1-	RX-
7	MDI3+	Reserved
8	MDI3-	Reserved

Table 1-6: PXIe-63987 Ethernet Port Pin Assignments

The Ethernet ports each include two LED indicators, one Active/Link indicator and one Speed indicator, functioning as follows.

	LED	Status	Description
	Active/Link (Yellow)	Off	Ethernet port is disconnected
		On	Ethernet port is connected with no data transmission
		Flashing	Ethernet port is connected with data transmitted/received
	Speed (Green/ Orange)	Off	10 Mbps
		Green	100 Mbps
		Orange	1000 Mbps

1.3.7 USB 3.0 Ports

The PXIe-63987 provides two Type A USB 3.0 ports on the front panel, supporting SuperSpeed, Hi-Speed, full-speed, and low-speed transmission for downstream. Multiple boot devices, including USB flash, USB external HD, and USB CD-ROM drives are supported, with boot priority configured in BIOS.

NOTE: USB 3.0 may not be supported by the OS installation programs/environment. Use USB 2.0 ports for OS installation if necessary.

1.3.8 COM Port

A COM port on the front panel with D-sub 9P connectors supports RS-232/RS-422/RS-485 by BIOS selection.

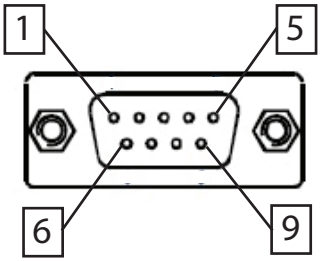


Figure 1-7: COM Port

Pin	Signal Name		
	RS-232	RS-422	RS-485
1	DCD#	TXD422-	485DATA-
2	RXD	TXD422+	485DATA+
3	TXD	RXD422+	N/S
4	DTR#	RXD422-	N/S
5	GND	N/S	N/S
6	DSR#	N/S	N/S
7	RTS#	N/S	N/S
8	CTS#	N/S	N/S
9	RI#	N/S	N/S

Table 1-7: D-Sub COM Port Signal Functions

1.3.9 Onboard Connections and Settings

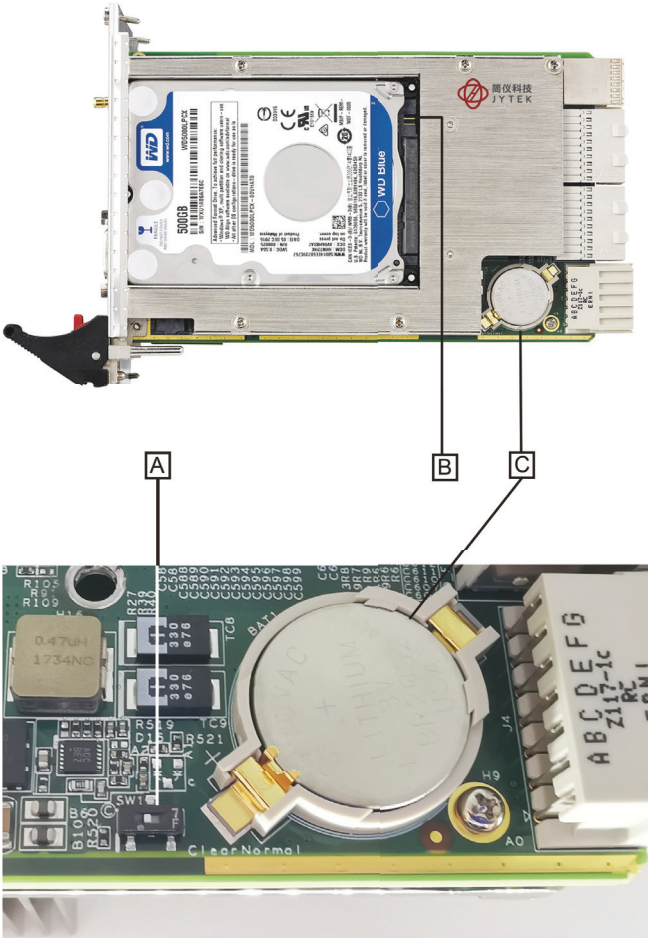


Figure 1-8: PXIe-63987 Onboard Configuration

A	Clear CMOS switch
B	SATA connector
C	System battery

Table 1-8: Onboard Configuration Legend

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2 Getting Started

This chapter describes procedures for installing the PXIe-63987 and making preparations for its operation, including hardware and software setup. Please note that the PXIe-63987 is shipped with RAM and HDD or SSD preinstalled. Please contact JYTEK or authorized dealer if there are any problems during the installation.

Diagrams and illustrated equipment are for reference only. Actual system configuration and specifications may vary.

2.1 Package Contents

Before beginning, check the package contents for any damage and ensure that the following items are included:

- PXIe-63987 Controller (equipped with RAM and HDD or SSD)

If any of these items are missing or damaged, contact the dealer from whom you purchased the product. Save the shipping materials and carton in case you want to ship or store the product in the future.

Do not install or apply power to equipment that is damaged or missing components. Retain the shipping carton and packing materials for inspection. Please contact your JYTEK dealer/vendor immediately for assistance and obtain authorization before returning any product.

2.2 Operating System Installation

For more detailed information about the operating system, refer to the documentation provided by the operating system manufacturer. Preferred/supported operating systems for PXIe-63987 are:

- Windows 10 64-bit
- For other OS support, please contact JYTEK

Most operating systems require initial installation from a hard drive, floppy drive, or CD-ROM drive. The PXIe-63987 controller supports USB CD-ROM drive, USB flash disk, USB external hard drive, or a USB floppy drive as the first boot device. Please see Section B.5.1: Boot Configura-

tion for information about setting the boot devices. These devices should be configured, installed, and tested with the supplied drivers before attempting to load the new operating system.


NOTE:

Read the release notes and installation documentation provided by the operating system vendor. Be sure to read all the README files or documents provided on the distribution disks, as these typically note documentation discrepancies or compatibility problems.

1. Select the appropriate boot device order from the BIOS Boot Setup Menu based on the OS installation media used. For example, if the OS is distributed on a bootable installation CD, select USB CD-ROM as the first boot device and reboot the system with the installation CD in the USB CD-ROM drive
2. Proceed with the OS installation as directed and be sure to select appropriate device types if prompted. Refer to the appropriate hardware manuals for specific device types and compatibility modes of JYTEK PXI products.
3. When installation is complete, reboot the system and set the boot device order in the SETUP boot menu accordingly.

2.2.1 Installation Environment

When preparing to install any equipment described in this manual, please refer to Important Safety Instructions.

Only install equipment in well lit areas on flat, sturdy surfaces with access to basic tools such as flat- and cross-head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

Recommended Installation Tools include:

- Phillips (cross-head) screwdriver
- Flat-head screwdriver
- Anti-static wrist strap
- Anti-static mat

JYTEK PXIe-63987 system controllers are electrostatically sensitive and can be easily damaged by static electricity. The equipment must

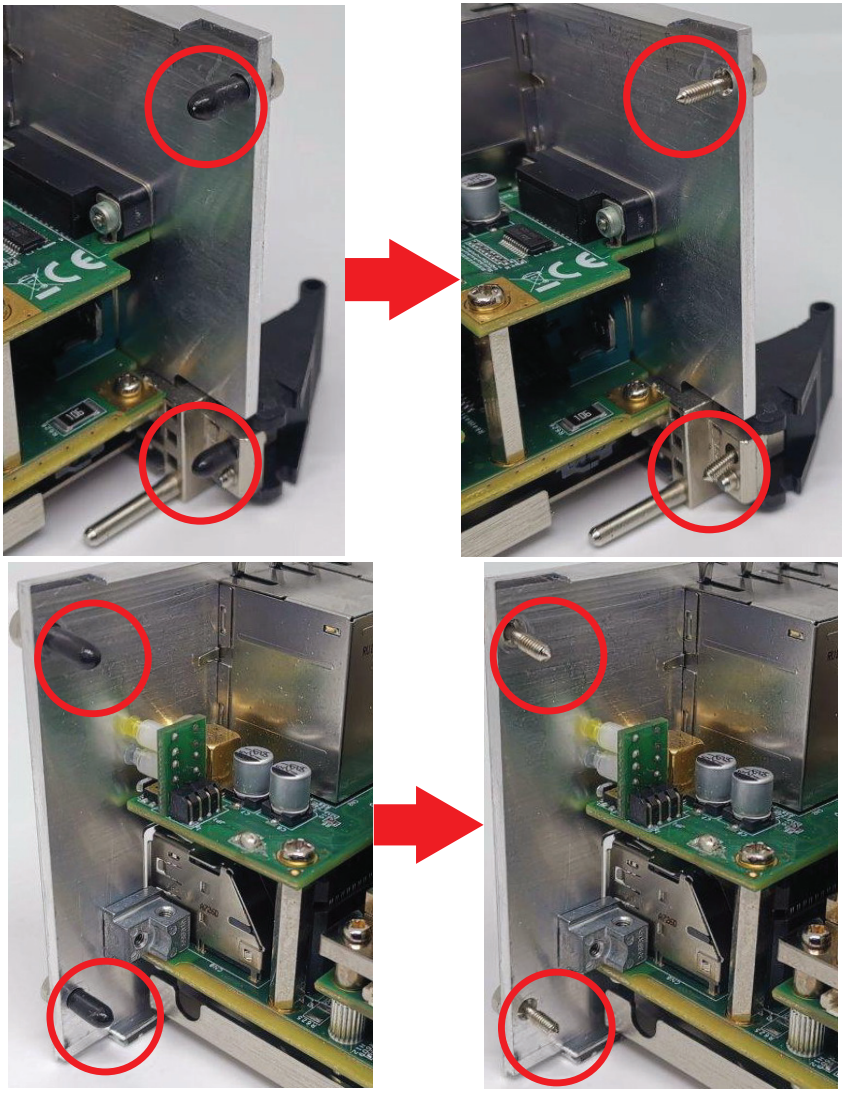
be handled on a grounded anti-static mat, and operators must wear an anti-static wristband, grounded at the same point as the anti-static mat.

Inspect the carton and packaging for damage. Shipping and handling may cause damage to the contents. Ensure that all contents are undamaged before installing.

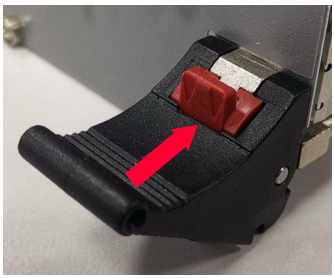
All equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing or installing.

2.2.2 Installing the PXIe-63987

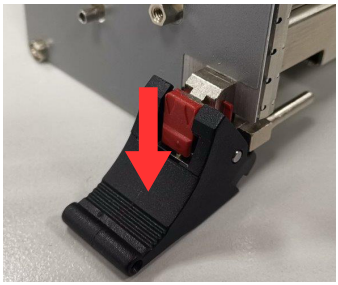
1. Remove all screw caps (x4).



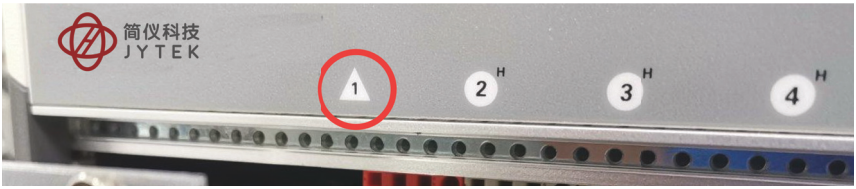
2. Release the red locking lever



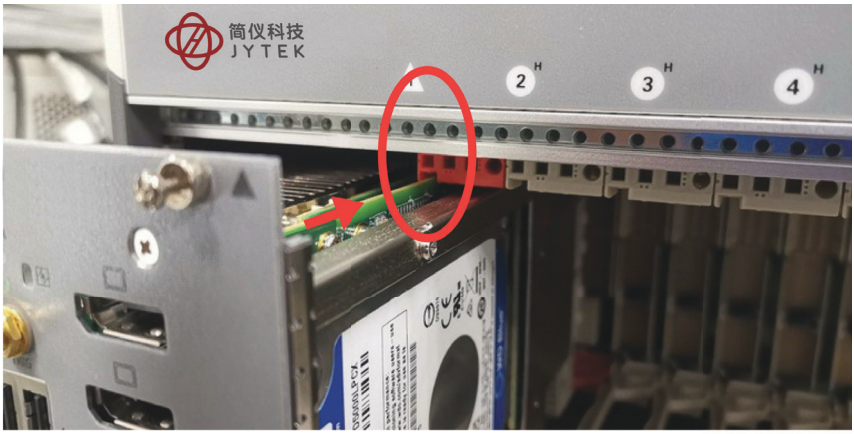
3. Depress the latch

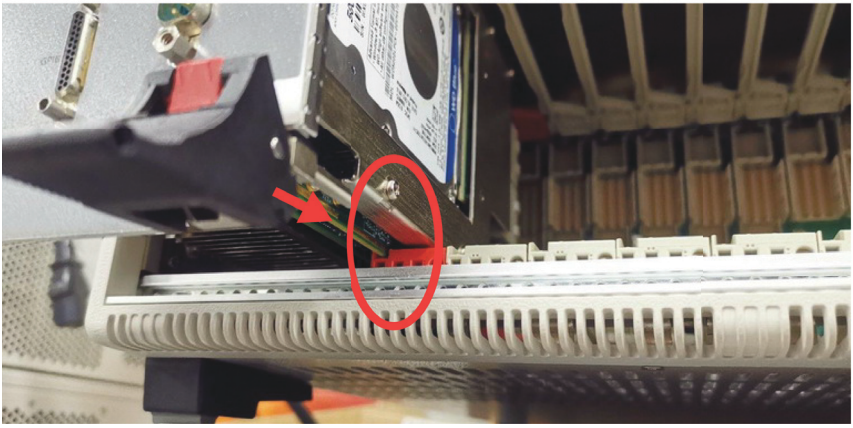


4. Locate the system controller slot of the chassis (Slot 1).



5. Align the controller's top and bottom edges with the card guides, and carefully slide the PXIe-63987 into the chassis, as shown



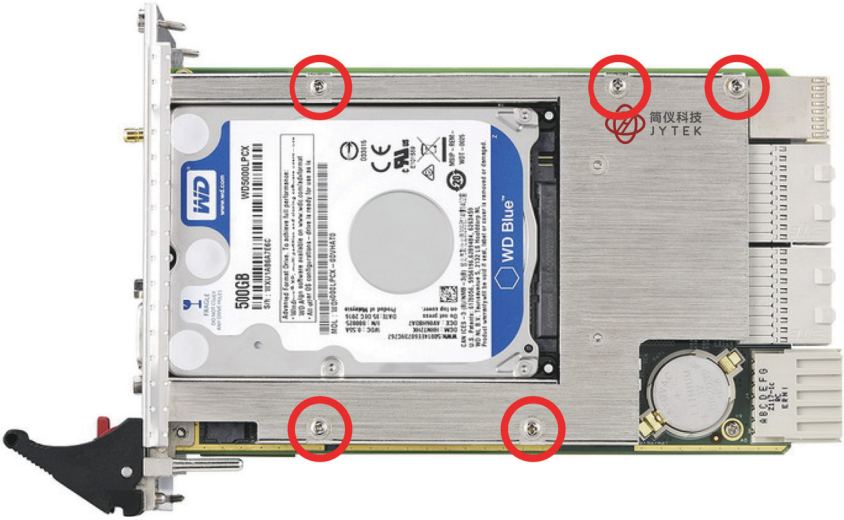


6. Elevate the latch until the PXIe-63987 is fully seated in the chassis backplane. The alignment pin on the rear of the latch can be threaded into the best fit alignment port in the chassis rail.
7. Fasten the four mounting screws on the faceplate and connect all peripheral devices.

2.2.3 Replacing the Hard Drive or Solid State Drive

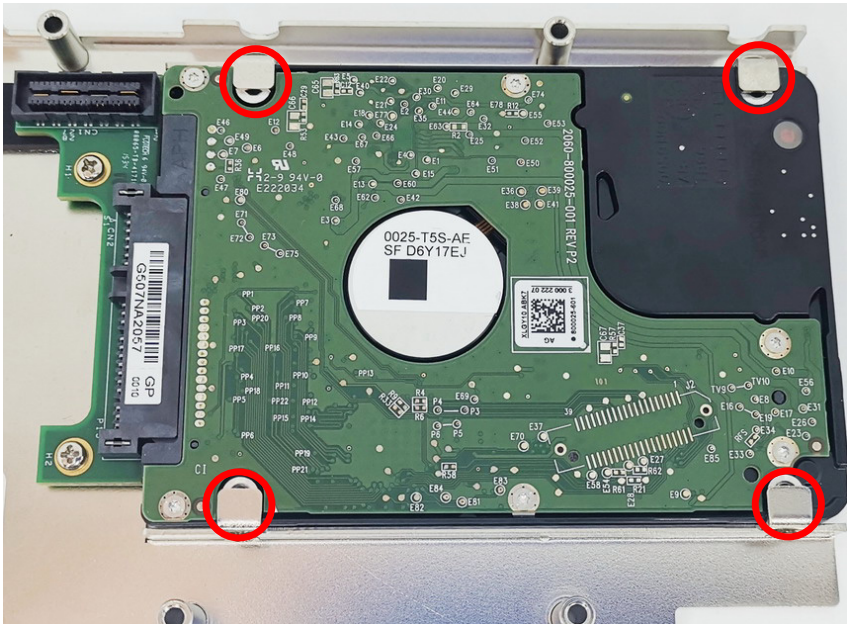
The PXIe-63987 provides a SATA 3.0 port with a pre-installed 2.5" SATA hard drive or solid state drive. Replacing the HDD or SSD is accomplished as follows.

1. Locate the five screws attaching the hard drive housing to the PXIe-63987 controller, as shown.



2. Remove the screws.
3. Gently lift and remove the housing with the installed HDD or SSD.
4. Locate the four screws (two on each side, as shown) fixing the

hard drive, and remove.



5. To install a HDD or SSD or other compatible SATA hard drive, reverse the steps and reinstall the PXIe-63987 into the PXI system.

2.2.4 Replacing the Battery Backup

The PXIe-63987 is provided with a 3.0 V “coin cell” lithium battery, replacement of which is as follows.

1. Turn off the PXI chassis.
2. Remove the PXIe-63987 embedded controller from the chassis. Observe all anti-static precautions.
3. To remove the battery, gently insert a small (approx. 5 mm) flathead screwdriver under the battery at the negative retaining clip. Gently pry up and the battery should easily pop out.
4. Place a fresh identical battery (CR2032 or equivalent) in the socket, ensuring that the positive pole (+) is facing upwards. The battery is most easily seated by first being inserted under the positive retaining clip, and then pushed downward at the

negative retaining clip. The battery should easily snap into position.

5. Reinstall the embedded controller into the PXI chassis and restore power.

2.2.5 Clearing CMOS

In the event of a system malfunction causing the PXIe-63987 to halt or fail to boot, clear the CMOS and restore the controller BIOS to its default settings. To clear the CMOS:

1. Shut down the controller operating system and turn off the PXI Chassis.
2. Remove the PXIe-63987 from the chassis. Observe all anti-static precautions.
3. Locate the CMOS clear switch (SW1) on the board (see Section 1.3.9: Onboard Connections and Settings). Move the switch from Normal position

to Clear position

and wait for 5 seconds, then return the switch to Normal position.

4. Remount the controller into the PXI chassis.
5. Press "Delete" or "ESC" to enter the BIOS setup when the splash logo appears.
6. Press "F9" to load Optimized defaults in BIOS setup
7. Modify the system date and time
8. Press "F10" to save configuration and exit

3 Driver Installation

Windows 10 carries most device drivers for the PXIe-63987, built-in. Others can be downloaded from the JYTEK PXIe-63987 Product Page.

After downloading, execute the Setup file, and follow the instructions to complete installation for the following drivers

- Intel® chipset driver
- Intel® graphics driver
- Intel® Ethernet driver
- Intel® RST driver
- Intel® ME driver
- GPIB driver
- PXI trigger I/O driver
- PXI platform service (for more information, please refer to the JYTEK PXI Platform Service Manual)

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Appendix A - PXI Trigger I/O Function Reference

This appendix describes use of the PXI trigger I/O function library for the PXIe-63987 controller, to program routing of trigger signals between the trigger I/O SMB connector on the faceplate and the PXI trigger bus on the backplane. API files are located in the installation directory of the PXI Trigger I/O driver.

A.1 Data Types

The PXIe-63987 library uses these data types in pxitrigio.h in the directory X:\ADLINK\PXI Trigger IO\Include. It is recommended that you use these data types in your application programs. The table shows the data type names, ranges, and corresponding data types in C/C++, Visual Basic, and Delphi for reference.

Type	Description	Range	Type		
			C/C++ (for 32-bit compiler)	Visual Basic	Pascal (Delphi)
U8	8-bit ASCII character	0 to 255	unsigned char	Byte	Byte
I16	16-bit signed integer	-32768 to 32767	short	Integer	SmallInt
U16	16-bit unsigned integer	0 to 65535	unsigned short	Not supported by BASIC, use the signed integer (I16) instead	Word
I32	32-bit signed integer	-2147483648 to 2147483647	long	Long	LongInt
U32	32-bit unsigned integer	0 to 4294967295	unsigned long	Not supported by BASIC, use the signed long integer (I32) instead	Cardinal
F32	32-bit single-precision floating-point	-3.402823E38 to 3.402823E38	float	Single	Single

Type	Description	Range	Type		
			C/C++ (for 32-bit compiler)	Visual Basic	Pascal (Delphi)
F64	64-bit double-precision floating-point	1.797683134862315E308 to 1.797683134862315E309	double	Double	Double

A.2 Function Library

This section provides detailed definitions of the functions available in the PXIe-63987 function library. Each function includes a description, list of supported cards, syntax, parameter list and Return Code information.

A.2.1 TRIG_Init

Description

Initializes trigger I/O function of PXIe-63987 controller. TRIG_Init must be called before the invocation of any other trigger I/O function.

Syntax

C/C++

```
I16 TRIG_Init()
```

Visual Basic

```
TRIG_Init As Integer
```

Parameter

None

Return Code

ERR_NoError
ERR_BoardBusy
ERR_OpenDriverFail
ERR_GetGPIOAddress

A.2.2 TRIG_Close

Description

Closes trigger I/O function of PXIe-63987 controller, releasing resources allocated for the trigger I/O function. Users must invoke TRIG_Close before exiting the application.

Syntax

C/C++

```
I16 TRIG_Close()
```

Visual Basic

```
TRIG_Close() As Integer
```

Parameter

None

Return Code

ERR_NoError
ERR_BoardNoInit

A.2.3 TRIG_SetSoftTrg

Description

Generates a TTL trigger signal to the trigger I/O SMB connector on the faceplate or the PXI trigger bus on the backplane by software command

Syntax

C/C++

```
I16 TRIG_SetSoftTrg(U8 Status)
```

Visual Basic

```
TRIG_SetSoftTrg (ByVal status As Byte) As Integer
```

Parameters

Status

Logic level of trigger signal.

Available value description:

0: Logic low

1: Logic high

Return Code

ERR_NoError
ERR_BoardNoInit

A.2.4 TRIG_Trigger_Route

Description

Routes the trigger signal between the trigger I/O SMB connector on the faceplate and the PXI trigger bus on the backplane. This function also allows routing of the software-generated trigger signal to SMB connector or trigger bus.

Syntax

C/C++

I16 TRIG_Trigger_Route (U32 source, U32 dest, U32 halfway)

Visual Basic

TRIG_Trigger_Route (ByVal source As Long, ByVal dest As Long, ByVal halfway As Long) As Integer

Parameters

source

Source of trigger routing. It can be one of the following values.

Available value	Description
PXI_TRIG_VAL_SMB	SMB connector on the faceplate
PXI_TRIG_VAL_SOFT	Software-generated trigger signal
PXI_TRIG_VAL_TRIG0	PXI trigger bus #0
PXI_TRIG_VAL_TRIG1	PXI trigger bus #1
PXI_TRIG_VAL_TRIG2	PXI trigger bus #2
PXI_TRIG_VAL_TRIG3	PXI trigger bus #3
PXI_TRIG_VAL_TRIG4	PXI trigger bus #4
PXI_TRIG_VAL_TRIG5	PXI trigger bus #5
PXI_TRIG_VAL_TRIG6	PXI trigger bus #6
PXI_TRIG_VAL_TRIG7	PXI trigger bus #7

dest

Destination of trigger routing. It can be one of the following values.

Available value	Description
PXI_TRIG_VAL_SMB	SMB connector on the faceplate
PXI_TRIG_VAL_TRIG0	PXI trigger bus #0
PXI_TRIG_VAL_TRIG1	PXI trigger bus #1
PXI_TRIG_VAL_TRIG2	PXI trigger bus #2
PXI_TRIG_VAL_TRIG3	PXI trigger bus #3
PXI_TRIG_VAL_TRIG4	PXI trigger bus #4
PXI_TRIG_VAL_TRIG5	PXI trigger bus #5
PXI_TRIG_VAL_TRIG6	PXI trigger bus #6
PXI_TRIG_VAL_TRIG7	PXI trigger bus #7

halfway

Halfway point of trigger routing. This parameter is used only to route the software-generated trigger signal to the SMB connector on the faceplate. In this case, the halfway should be set as one of the trigger bus lines, otherwise as PXI_TRIG_VAL_NONE.

Available value	Description
PXI_TRIG_VAL_NONE	No halfway point
PXI_TRIG_VAL_TRIG0	PXI trigger bus #0
PXI_TRIG_VAL_TRIG1	PXI trigger bus #1
PXI_TRIG_VAL_TRIG2	PXI trigger bus #2
PXI_TRIG_VAL_TRIG3	PXI trigger bus #3
PXI_TRIG_VAL_TRIG4	PXI trigger bus #4
PXI_TRIG_VAL_TRIG5	PXI trigger bus #5
PXI_TRIG_VAL_TRIG6	PXI trigger bus #6
PXI_TRIG_VAL_TRIG7	PXI trigger bus #7

Return Code

ERR_NoError
ERR_BoardNoInit
ERR_Set_Path

A.2.5 TRIG_Trigger_Clear

Description

Clears the trigger routing setting

Syntax

C/C++

```
I16 TRIG_Trigger_Clear()
```

Visual Basic

```
TRIG_Trigger_Clear() As Integer
```

Parameters

None

Return Code

ERR_NoError
ERR_BoardNoInit
ERR_Trigger_Clr

A.2.6 TRIG_GetSoftTrg

Description

Acquires the current software trigger state, with default state after system boot of Logic Low

Syntax

C/C++

```
I16 TRIG_GetSoftTrg(U8 *Status)
```

Visual Basic

```
TRIG_GetSoftTrg (status As Byte) As Integer
```

Parameters

Status

Returns the logic level of software trigger signal

Returned value:

0: Logic low

1: Logic high

Return Code

ERR_NoError
ERR_BoardNoInit
ERR_Query_Status

A.2.7 TRIG_Trigger_Route_Query

Description

Acquires the current trigger signal routing path

Syntax

C/C++

I16 TRIG_Trigger_Route_Query (U32* source, U32* dest, U32* halfway)

Visual Basic

TRIG_Trigger_Route_Query (source As Long, dest As Long, halfway As Long) As Integer

Parameters

source

Returns to the current source of trigger routing, with possible values including:

Available Definition	Defined Value
PXI_TRIG_VAL_NONE	0
PXI_TRIG_VAL_SMB	2
PXI_TRIG_VAL_SOFT	3
PXI_TRIG_VAL_TRIG0	111
PXI_TRIG_VAL_TRIG1	112
PXI_TRIG_VAL_TRIG2	113
PXI_TRIG_VAL_TRIG3	114
PXI_TRIG_VAL_TRIG4	115
PXI_TRIG_VAL_TRIG5	116
PXI_TRIG_VAL_TRIG6	117
PXI_TRIG_VAL_TRIG7	118

dest

Returns to the current destination of trigger routing, with possible values including:

Available Definition	Defined Value
PXI_TRIG_VAL_NONE	0
PXI_TRIG_VAL_SMB	2
PXI_TRIG_VAL_TRIG0	111
PXI_TRIG_VAL_TRIG1	112
PXI_TRIG_VAL_TRIG2	113
PXI_TRIG_VAL_TRIG3	114
PXI_TRIG_VAL_TRIG4	115
PXI_TRIG_VAL_TRIG5	116
PXI_TRIG_VAL_TRIG6	117
PXI_TRIG_VAL_TRIG7	118

halfway

Returns to the current halfway point of trigger routing, with possible values including:

Available Value	Description
PXI_TRIG_VAL_NONE	0
PXI_TRIG_VAL_TRIG0	111
PXI_TRIG_VAL_TRIG1	112
PXI_TRIG_VAL_TRIG2	113
PXI_TRIG_VAL_TRIG3	114
PXI_TRIG_VAL_TRIG4	115
PXI_TRIG_VAL_TRIG5	116
PXI_TRIG_VAL_TRIG6	117
PXI_TRIG_VAL_TRIG7	118

Return Code

ERR_NoError
ERR_BoardNoInit
ERR_Query_Status

A.2.8 TRIG_GetDriverRevision

Description

Acquires the PXI Trigger software driver version; format of the version number is major.minor1.minor2

Syntax

C/C++

I16 TRIG_GetDriverRevision(unsigned short *major, unsigned short *minor1, unsigned short *minor2)

Visual Basic

TRIG_GetDriverRevision (major As Integer, minor1 As Integer, minor2 As Integer) As Integer

Parameters

major

Returns the major version number of the pxi trigger software driver

minor1

Returns the first minor version number of the pxi trigger software driver

minor2

Returns the second minor version number of the pxi trigger software driver

Return Code

ERR_NoError
ERR_Query_Revision

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Appendix B BIOS Setup

B.1 Menu Structure

This section presents the primary menus of the BIOS Setup Utility. Use the following table as a quick reference for the contents of the BIOS Setup Utility. The subsections in this section describe the submenus and setting options for each menu item. The default setting options are presented in **bold**, and the function of each setting is described in the right hand column of the respective table.

Main	BIOS Information Processor Information PCH Information System Management ? System Date and Time
Advanced	CPU? Graphics? USB Configuration? Onboard Devices Configuration? PCI and PCIe Configuration? Advanced Power Management? Network Stack Configuration? Intel I210? Intel I219-LM? Hardware Health Configuration? PXIe Links Control Configuration?
Security	Password Description? Administrator Password? User Password? Secure Boot?
Boot	Boot Configuration? CSM Configuration? Fixed Boot Order Priorities?
Save & Exit	Save Options? Default Options? Boot Override?


NOTE:

? indicates a submenu

B.2 Starting the BIOS

1. Power on or reboot the PXIe-63987 controller.
2. Press the <Delete> key when the controller beeps. This should be concurrent with the main startup screen. The BIOS setup program loads after a short delay.
3. The Main menu is displayed when you first enter the BIOS setup program.


NOTE:

In most cases, the < Delete > key is used to invoke the setup screen. There are several cases that use other keys, such as < F1 >, < F2 >, and so on.

The main BIOS setup menu is the first screen that you can navigate. Each main BIOS setup menu option is described in this user's guide.

The Main BIOS setup menu screen has two main frames. The left frame displays all the options that can be configured. "Grayed" options cannot be configured, "Blue" options can be.

The right frame displays the key legend. Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

Navigation

The BIOS setup/utility uses a key-based navigation system called hot keys. Most BIOS setup utility hot keys can be used at any time during setup navigation, as follows.

Key(s)	Function
Right Arrow, Left Arrow	Moves between different setup menus
Up Arrow, Down Arrow	Moves between options within a setup menu
<Enter>	Opens a submenu or displays all available settings for a highlighted configuration option
<Esc>	Returns to the previous menu and shortcuts to the Exit menu from top-level menus
<+> and <–>	Cycles between all available settings
<Tab>	Selects time and date fields
<F1>	Opens the general help window for the BIOS
<F2>	Loads previous values into the BIOS
<F3>	Restores optimal default values into the BIOS
<F4>	Saves the current configuration and exits BIOS setup

Table B-1: BIOS Hot Key Functions

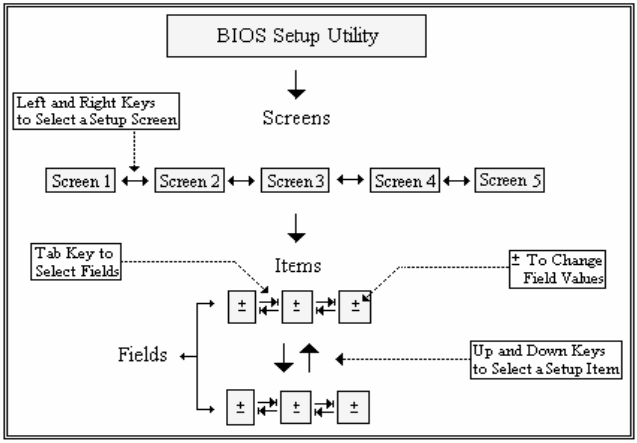

Figure B-1: BIOS Setup Navigation


NOTE:

A hot key legend is located in the right frame on most setup screens.

The < F8 > key on your keyboard is the Fail-Safe key. It is not displayed on the key legend by default. To set the Fail-Safe settings of the BIOS, press the < F8 > key on your keyboard. It is located on the upper row of a standard 101 keyboard. The Fail-Safe settings allow the motherboard to boot up with the least amount of options set. This can lessen the probability of conflicting settings.

B.3 Main

The Main Menu provides read-only information about your system and also allows you to set the System Date and Time. Refer to the tables below for details of the submenus and settings.

B.3.1 BIOS Information

Feature	Options	Description
BIOS Vendor	Info only	American Megatrends
Core Version	Info only	Displays Core version
Compliancy	Info only	Displays compliance information
Project Version	Info only	JYTEK BIOS version
Build Date and Time	Info only	Date the JYTEK BIOS was built
Access Level	Info only	Current BIOS menu access permission
Link Cap	Info only	PCI Express link configuration to PXIe chassis. 2 link configuration : x8 x16 4 link configuration : x4 x4 x4 x4

B.3.2 Processor Information

Feature	Options	Description
Name	Info only	Displays CPU brand name
CPU Signature	Info only	Displays CPU signature
CPU Speed	Info only	Displays CPU frequency
Processor ID	Info only	Displays CPU ID
Stepping	Info only	Displays CPU stepping
Number of Processors	Info only	Displays number of processors
GT Info	Info only	Displays GT info of Intel Graphics.
GOP Version	Info only	Graphics Output Protocol version
Memory RC Version	Info only	Displays memory version
Total Memory	Info only	Displays installed memory size
Memory Frequency	Info only	Displays memory frequency

B.3.3 PCH Information

Feature	Options	Description
Name	Info only	Displays PCH name.
PCH SKU	Info only	Displays PCH SKU
Stepping	Info only	Displays PCH stepping
LAN PHY Revision	Info only	Displays LAN PHY revision
ME FW Version	Info only	Displays version of ME
ME Firmware SKU	Info only	Displays ME Firmware Kit SKU number

B.3.4 System Management

Board Information

Board Information	Info only	Description
SEMA Firmware	Read only	Displays SEMA firmware

Board Information	Info only	Description
Build Date	Read only	Displays SEMA firmware build date
SEMA Boot loader	Read only	Displays SEMA boot loader
Build Date	Read only	Displays SEMA boot loader build date
Hardware Version	Read only	Displays SEMA hardware version
Serial Number	Read only	Displays SEMA S/N
Manufacturing Date	Read only	Displays SEMA manufacture date
Last Repair Date	Read only	Displays last SEMA repair date
MAC ID	Read only	Displays SMC MAC ID

Temperatures

Feature	Options	Description
Temperatures	Info only	
CPU Temperature	Info only	
Current	Read only	Displays current CPU temperature
Startup	Read only	Displays CPU startup temperature
Min	Read only	Displays min. CPU temperature
Max	Read only	Displays max. CPU temperature
Board Temperatures	Info only	
Current	Read only	Displays current board temperature
Startup	Read only	Displays board startup temperature
Min	Read only	Displays min. board temperature
Max	Read only	Displays max. board temperature

Power Consumption

Feature	Options	Description
Power Consumption	Info only	
Current Input Current	Read only	Displays input current
Current Input Power	Read only	Displays input power
VCORE	Read only	Displays actual voltage of the VCC_CORE
VGFX	Read only	Displays actual voltage of the VGFX
VMEM	Read only	Displays actual voltage of the VMEM
5VSB	Read only	Displays actual voltage of the 5VSB
VIN	Read only	Displays actual voltage of the VIN
5V	Read only	Displays actual voltage of the 5V
3.3V	Read only	Displays actual voltage of the 3.3V
3.3VSB	Read only	Displays actual voltage of the 3.3VSB

Runtime Statistics

Feature	Options	Description
Runtime Statistics	Info only	
Total Runtime	Read only	The returned value specifies the total time in minutes the system is running in S0 state
Current Runtime	Read only	The returned value specifies the time in seconds the system is running in S0 state, where the counter is cleared when the system is removed from the external power supply
Power Cycles	Read only	The returned value specifies the number of times the external power supply has been shut down
Boot Cycles	Read only	Boot count is increased after a HW- or SW-Reset or successful power-up
Boot Reason	Read only	Shows the event responsible for reboot of the system

Flags

Feature	Options	Description
Flags	Info only	
BMC Flags	Read only	
BIOS Select	Read only	Displays the current selection of BIOS ROM
ATX/AT-Mode	Read only	Displays ATX/AT mode
Exception Code	Read only	System exception reason

Power Up

Feature	Options	Description
Power Up	Info only	
Power-up Mode (only in effect if the module is in ATX-Mode)	Turn on **Remain off** Last State	Turn On: The machine starts automatically when the power supply is turned on. Remain Off: To start the machine the power button has to be pressed. Last State: when powered on during a power failure the system will automatically power on when power is restored

System Date and Time

Feature	Options	Description
System Date	Weekday, MM/DD/YYYY	Requires alpha-numeric entry of the day of the week, day of the month, calendar month, and all 4 digits of the year, indicating the century and year (Fri XX/XX/20XX)
System Time	HH/MM/SS	Presented as a 24-hour clock in hours, minutes, and seconds

B.4 Advanced

Provides settings for most user interfaces in the system.

B.4.1 CPU

Feature	Options	Description
CPU	Info only	Manufacturer, model, speed
CPU Signature	Info only	Displays CPU signature
Microcode Revision	Info only	Displays microcode revision
CPU Speed	Info only	Displays CPU operating frequency
Processor Cores	Info only	Displays Processor Cores
Hyper Threading Technology	Info only	Displays presence/absence of Intel Hyper Threading support
VMX	Info only	Displays presence/absence of Intel Virtualization Technology support
SMX/TXT	Info only	Displays presence/absence of Intel SMX Technology support
L1 Data Cache		Displays cache info
L1 Instruction Cache	Info only	Displays cache info
L2 Cache	Info only	Displays cache info
L3 Cache	Info only	Displays cache info
L4 Cache	Info only	Displays cache info
Hyper-Threading	Disabled **Enabled**	Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and disabled for other OS (not optimized). When Disabled only one thread per enabled core is active.
VT-d	Disabled **Enabled**	Enables/disables VT-d function on MCH
Intel (VMX) Virtualization Technology	Disabled **Enabled**	Enables/disables support for Intel Virtualization technology
Intel® SpeedStep(TM)	**Disabled** Enabled	Allows support for more than two frequency ranges

Feature	Options	Description
Turbo Mode	Disabled **Enabled**	Enables/disables turbo mode
Configurable TDP Boot Mode	**TDP Nominal** TDP Down Disabled	Configures TDP Mode as Nominal/Down/Disabled, where Disabled sets MSR to Nominal and MMI/O to Zero
Configurable TDP Lock	**Disabled** Enabled	Configurable TDP Mode Lock sets the Lock bits on TURBO_ACTIVATION_RATI/O and CONFIG_TDP_CONTROL When CTDP Lock is enabled, Custom ConfigTDP Count defaults to 1 and Custom ConfigTDP Boot Index to 0
Custom Configurable TDP	**Disabled** Enabled	Custom Configurable TDP settings
CPU C state	Disabled **Enabled**	Enables/disables CPU C states
Package C State limit	**Auto** C2 C3 C6 C7 Auto	Maximum Package C State limit
Intel Trusted Execution Technology	**Disabled** Enabled	Enables/disables Intel Trusted Execution Technology
DTS SMM	Disabled **Enabled**	Enables/disables CPU DTS
ACPI T-states	**Disabled** Enabled	Enables/disables ACPI 3.0 T-states

B.4.2 Memory Configuration

Feature	Options	Description
Memory RC Version	Info only	Displays Memory Reference Code version
Memory Frequency	Info only	Displays memory frequency
Total Memory	Info only	Displays total memory
DIMM#0/1	Info only	Displays DIMM#0/1
Memory Timings (tCL-tRCD-tRP-tRAS)	Info only	Displays memory timings

B.4.3 Graphics Configuration

Feature	Options	Description
GTT Size	2MB 4MB **8MB**	Selects Graphics Translation Table size
Aperture Size	128MB **256MB** 512M 1024MB 2048MB 4096MB	Selects Aperture size.
DVMT Pre-Allocated	0MB **32MB** 64MB	Selects DVMT Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device
DVMT Total Gfx Mem	128MB **256MB** MAX	Selects DVMT Total Graphics Memory size used by the Internal Graphics Device

B.4.4 Onboard Devices Configuration

Feature	Options	Description
Serial Port Configuration	Info only	
COM Device Settings	Info only	Serial port I/O address and IRQ

Feature	Options	Description
COM Control	**RS232** RS422 RS485	Selects serial port mode, from among RS232, RS422, and RS485
LAN Port Configuration	Info only	
LAN1 Controller	**Enabled** Disabled	Enables/disables onboard I219 LAN controller
LAN2 Controller	**Enabled** Disabled	Enables/disables onboard I210 LAN controller
SATA Configuration	Info only	
SATA Controller(s)	**Enabled** Disabled	Enables/disables SATA device
SATA Signal Setting	**HDD** SSD	Sets SATA signaling for optional HDD and SSD
Serial ATA Port X	Info only	Installed SATA device name
Software Preserve	Info only	Bootable OS in installed SATA device
Port X	Disabled **Enabled**	Enables/disables SATA port
Hot Plug	Disabled **Enabled**	Designates the port as Hot Pluggable

B.4.5 USB Configuration

Feature	Options	Description
USB Configuration	Submenu	
USB Module Version	Info only	
USB Devices	Info only	Lists USB-connected peripheral devices
Legacy USB Support	**Enabled** Disabled Auto	Enables legacy USB support, where Auto disables legacy support if no USB devices are connected, and Disable retains USB devices only for EFI applications and setup
XHCI Hand-off	**Enabled** Disabled	A workaround for OS without XHCI hand-off support. XHCI ownership change should be claimed by the XHCI OS driver
USB Mass Storage Driver Support	**Enabled** Disabled	Enables/disables USB Mass Storage driver support
Port 60/64 Emulation	Enabled **Disabled**	Enables I/O port 60h/64h emulation, and should be enabled for complete USB keyboard legacy support for non-USB aware OS
Device reset time-out	10 sec **20 sec** 30 sec 40 sec	USB mass storage device Start Unit command timeout
Device power-up delay	**Auto** Manual	Maximum time before the device properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port, 100 ms, for a Hub port the delay is taken from the Hub descriptor

B.4.6 Network Stack Configuration

Feature	Options	Description
Network Stack	Enabled **Disabled**	Enables/disables UEFI network stack.
IPv4 PXE Support	Enabled **Disabled**	Enables/disables IPv4 PXE boot support.
IPv6 PXE Support	Enabled **Disabled**	Enables/disables IPv6 PXE boot support.

Feature	Options	Description
PXE boot wait time	**0 sec**	Wait time for ESC key to abort PXE boot

B.4.7 PCI and PCIe Configuration

Feature	Options	Description
Above 4G Decoding	**Disabled** Enabled	Enables/disables Memory Mapped I/O BIOS assignment above 4GB.
Holdoff timer	**0**,1,2,3,4,5, 6,7,8 sec	System delay for PCI Express Discovery
Native PCIe Enable	**Disabled** Enabled	Enables/disables native PCIe
PEG Port Configuration	Info only	
PEG 0:1:0	Info only	Information about PCI express mode and link to the PCI Express bus root.
Max Link Speed	**Auto** Gen1 Gen2 Gen3	Sets maximum PCI Express link capability of the PCI Express bus root

B.4.8 Advanced Power Management

Feature	Options	Description
Advanced Power Management	Info only	
RTC Wake system from S5	**Disabled** Fixed Time Dynamic Time	Enables/disables system wake on alarm event, from among Fixed Time, where system wakes at the setting time, and Dynamic Time, in which system wakes at setting time later
PCIe Wake	Enabled **Disabled**	Enables/disables PCI Express bus and onboard LAN2 Controller (I210) wake capability
I219 LAN Wake	Enabled **Disabled**	Enables/disables onboard LAN1 Controller (I219) wake capability

B.4.9 Intel® I210 Gigabit Network Connection- (MAC address)

Feature	Options	Description
NIC Configuration	Submenu	
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	LAN port speed
Wake On LAN	**Enabled** Disabled	Enables/disables wake by receiving magic packet
Blink LEDs	Enter	Identifies physical network port by pressing to blink the LED of LAN port
UEFI Driver	Info only	UEFI driver version
Device Name	Info only	LAN port device name
Chip Type	Info only	LAN chip model
Link Status	Info only	LAN port link status
MAC Address	Info only	LAN port MAC address

B.4.10 Intel® Ethernet Connection (H) I219-LM - (MAC address)

Feature	Options	Description
NIC Configuration	Submenu	
Link Speed	**Auto Negotiated** 10 Mbps Half 10 Mbps Full 100 Mbps Half 100 Mbps Full	LAN port speed
Wake On LAN	**Enabled** Disabled	Enables/disables wake by receiving magic packet
Blink LEDs	Enter	Identifies physical network port by pressing to blink the LED of LAN port
UEFI Driver	Info only	UEFI driver version
Device Name	Info only	LAN port device name
Chip Type	Info only	LAN chip model

Feature	Options	Description
Link Status	Info only	LAN port link status
MAC Address	Info only	LAN port MAC address

B.4.11 System Health Status

Feature	Options	Description
System Health Status	Info only	
Ambient temp of PCIe switch	Info only	Ambient temperature near PCIe switch
Core temp of PCIe switch	Info only	Core temperature of PCIe switch
+3.3V(System)	Info only	System +3.3V voltage
+5V(System)	Info only	System +5V voltage
+12V(System)	Info only	System +12V voltage
VBAT	Info only	Battery voltage

B.4.12 PXIe Links Control Configuration

Feature	Options	Description
Link Configuration	Info only	PCI Express link configuration to PXIe chassis
Link 1 Width, Speed	Info only	Link lanes and mode
Max Link Speed	**Auto** Gen1 Gen2 Gen3	Maximum PCI Express link mode for Link 1
Link 2 Width, Speed	Info only	Link lanes and mode
Max Link Speed	**Auto** Gen1 Gen2 Gen3	Maximum PCI Express link mode

B.5 Boot

B.5.1 Boot Configuration

Feature	Options	Description
Boot Configuration	Info only	
Setup Prompt Timeout	**1**	Enables/disables onboard SATA controllers
Bootup NumLock State	**On**	Selects keyboard NumLock state at boot
Quiet Boot	Disabled **Enabled**	Enables/disables PATA port, enabling/disabling the SATA channel to which the onboard SATA to PATA converter is attached. When Enabled, system boot is delayed for the time specified in PATA Port Detection Timeout if no PATA device is connected, and Auto scans for PATA device and enables by default.
CSM Configuration	Submenu	
Fast Boot	**Disabled** Enabled	Defines the maximum time to wait for drive detection on PATA port
Boot Mode Select	UEFT Legacy	
Boot Option Priorities	Info only	

B.5.2 CSM Configuration

Feature	Options	Description
CSM Support	Enabled **Disable**	Determines whether CSM will launch
CSM16 Module Version	Info only	
GateA20 Active	**Upon Request** Always	Selected from among UPON REQUEST, in which GA20 can be disabled using BIOS services, and ALWAYS, in which GA20 cannot be disabled, useful when any RT code is executed above 1MB
INT19 Trap Response	**Immediate** Postponed	BIOS reaction on INT19 trapping by Option ROM, where IMMEDIATE executes trap immediately and POSTPONED executes trap during legacy boot
Boot Option filter	**UEFI and Legacy** Legacy only UEFI only	Controls to which devices the system can boot
Option ROM execution	Info only	
Network	**Do not launch** Legacy only UEFI only	Controls execution of UEFI and Legacy PXE OpROM.
Storage	Do not launch **UEFI** Legacy only	Controls execution of UEFI and Legacy Storage OpROM.
Video	Do not launch **UEFI** Legacy only	Controls execution of UEFI and Legacy Video OpROM
Other PCI devices	**UEFI** Legacy OpROM	For PCI devices other than Network, Mass storage or Video, defines the OpROM to launch.

B.6 Security

B.6.1 Password Description

Feature	Options	Description
Administrator Password	Enter password	
User Password	Enter password	
Attempt Secure Boot		
Attempt Secure Boot	**Disable** Enable	Enables/disables
Password Description If ONLY the Administrator's password is set, then this only limits access to BIOS setup menu and is only asked for when entering BIOS setup menu. If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter BIOS setup menu. In BIOS setup menu the User will have Administrator rights.		

B.7 Save & Exit

Feature	Options	Description
Save Options	Info only	
Save Changes and Exit		Saves changes and exits system setup
Discard Changes and Exit		Discards changes and exits system setup
Save Changes and Reset		Saves changes and resets system
Discard Changes and Reset		Discards changes and resets system
Save Changes		Save changes made so far to Setup options
Discard Changes		Discards Changes made so far to Setup options
Default Options	Info Only	
Restore Defaults		Restores/loads Default values for all Setup options
Save as User Defaults		Saves changes made so far as User Defaults
Restore User Defaults		Restores User Defaults to all Setup options

Feature	Options	Description
Boot Override	Info Only	
Launch EFI Shell from filesystem device		Attempts to launch EFI shell application (shell.efi) from an available filesystem device

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Appendix C Dual BIOS

Dual BIOS is a backup function that maintains normal operation of the PXIe system module when unexpected boot failure occurs under the default BIOS. Dual BIOS consists of a main BIOS, a backup BIOS, and an independent controller. In normal boot, the main BIOS powers on and boots the system into the OS, monitored by the independent controller. If the main BIOS malfunctions, for example, as the result of corruption incurred by a failed update, boot procedure is terminated abnormally. The backup BIOS is then activated automatically to perform boot procedure. When backup BIOS is activated, during BIOS power-on, notifications are generated indicating that backup BIOS has been deployed. To restore main BIOS function, contact technical support.

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Appendix D Legacy Boot Mode Settings

UEFI boot mode is default for the PXIe-63987 BIOS.

To boot in legacy boot mode, change related settings in BIOS menu:

1. Power on and press DEL or ESC to enter BIOS menu
2. Move to Boot
3. Under “Boot mode select” select “LEGACY”
4. Move to Boot, CSM
5. Under “CSM Support” select “Enabled”
6. Under “Network” select “Legacy”
7. Under “Storage” select “Legacy”
8. Under “Video” select “Legacy”
9. Under “Other PCI devices” select “Legacy”
10. Press F10 and Enter to save and exit BIOS menu. The system will restart and apply settings for Legacy boot mode.

To restore UEFI boot mode:

1. Power on and press DEL or ESC to enter BIOS menu
2. Press F9 and Enter to load optimized defaults
3. Press F10 and Enter to save and exit BIOS menu

The system restarts and default settings for UEFI boot mode are applied.

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Important Safety Instructions

For user safety, please read and follow all instructions, Warnings, Cautions, and Notes marked in this manual and on the associated device before handling/operating the device, to avoid injury or damage.

S'il vous plaît prêter attention stricte à tous les avertissements et mises en garde figurant sur l'appareil , pour éviter des blessures ou des dommages.

- Read these safety instructions carefully
- Keep the User's Manual for future reference
- Read the Specifications section of this manual for detailed information on the recommended operating environment
- The device can be operated at an ambient temperature of 50ºC
- When installing/mounting or uninstalling/removing device; or when removal of a chassis cover is required for user servicing (See "Getting Started" on page 21):
  - Turn off power and unplug any power cords/cables
  - Reinstall all chassis covers before restoring power
- To avoid electrical shock and/or damage to device:
  - Keep device away from water or liquid sources
  - Keep device away from high heat or humidity
  - Keep device properly ventilated (do not block or cover ventilation openings)
  - Always use recommended voltage and power source settings
  - Always install and operate device near an easily accessible electrical outlet
  - Secure the power cord (do not place any object on/over the power cord)
  - Only install/attach and operate device on stable surfaces and/or recommended mountings
- If the device will not be used for long periods of time, turn off and unplug from its power source
- Never attempt to repair the device, which should only be serviced by qualified technical personnel using suitable tools

- A Lithium-type battery may be provided for uninterrupted backup or emergency power.

Risk of explosion if battery is replaced with one of an incorrect type; please dispose of used batteries appropriately.
Risque d'explosion si la pile est remplacée par une autre de type incorrect. Veuillez jeter les piles usagées de façon appropriée.

- The device must be serviced by authorized technicians when:
  - The power cord or plug is damaged
  - Liquid has entered the device interior
  - The device has been exposed to high humidity and/or moisture
  - The device is not functioning or does not function according to the User's Manual
  - The device has been dropped and/or damaged and/or shows obvious signs of breakage
- Disconnect the power supply cord before loosening the thumbscrews and always fasten the thumbscrews with a screwdriver before starting the system up
- It is recommended that the device be installed only in a server room or computer room where access is:
  - Restricted to qualified service personnel or users familiar with restrictions applied to the location, reasons therefor, and any precautions required
  - Only afforded by the use of a tool or lock and key, or other means of security, and controlled by the authority responsible for the location

	**BURN HAZARD** Touching this surface could result in bodily injury. To reduce risk, allow the surface to cool before touching. ***RISQUE DE BRÛLURES*** *Ne touchez pas cette surface, cela pourrait entraîner des blessures.* *Pour éviter tout danger, laissez la surface refroidir avant de la toucher.*

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Getting Service

Customer satisfaction is our top priority. Contact us should you require any service or assistance.

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